Three Topologies of Transformer-less High-Gain Step-up Luo Converter for Renewable Energy Applications

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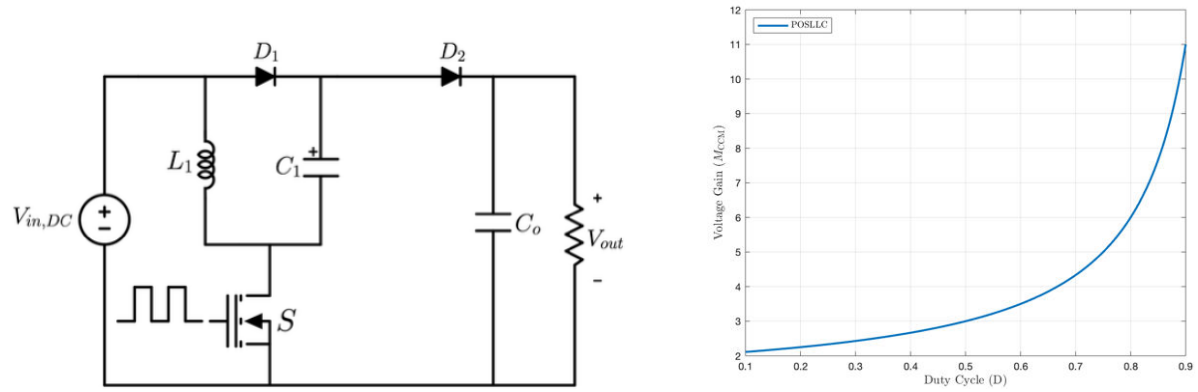
Abstract:
This article introduces three proposed topologies, each an extension of the conventional DC-DC positive output super lift Luo converter (POSLLC). By incorporating a switched-inductor (SL) cell into the POSLLC, the three modified POSLLC topologies succeed to provide a high output voltage along with a significant voltage gain. A high-voltage gain DC-DC converter is a crucial element in renewable energy systems, particularly in photovoltaic (PV) applications. It boosts the voltage before the converter is connected to a DC load or an AC load through an inverter, since the output voltage from a PV module is relatively low. The proposed designs provide several favorable features, including the utilization of only one controlled switch, continuous input current, the availability of common ground between the input and output, and the generation of a positive output voltage polarity. The proposed three topologies can provide a voltage gain of 8, 14, and 15, in comparison with only 5 in the original POSLLC when the duty cycle is 75%. MATLAB/Simulink models were developed and simulated to evaluate the consistency of the theoretical results obtained.

Key words*: high voltage gain, DC-DC converters, switched-inductor, renewable energy applications.*

1. INTRODUCTION

Several applications require a portable and compact high-voltage devices, such as X-ray machines, water treatment, and food processing. In general, these portable high voltage devices are powered by sources that have low voltage ratings, such as solar photovoltaic (PV), fuel cell, or battery. Because these sources have low voltage ratings, a large gain DC-DC converter is essential in order to boost the voltage rating across the load (Kumaravel and Babu 2022). Although traditional step-up DC-DC converters, such as the boost converter, Zeta converter, SEPIC converter, and positive output super lift Luo converter (POSLLC) have a simple structure, reduction in cost and size, and higher efficiency, their voltage gain is low when operated at duty cycles less than one. Figure 1 illustrates the circuit layout, and the voltage gain as a function of duty cycle of the POSLLC. The voltage gain equation of the POSLLC is expressed in (1), where *"d"* refers to duty cycle. The POSLLC maintains a voltage gain of eleven at a duty cycle of 0.9, which is considered a very high duty cycle, as can be seen in Figure 2. Operating the converters at such high duty cycles above 85% can cause many negative issues, such as reverse recovery problems, higher voltage and current stress across switches, lower efficiency, and poor voltage gain (Rahimi et al. 2021). According to Gholizadeh, Gorji, and Sera (2024, p. 1535), it has been shown practically that operating the conventional DC-DC converters, especially the SEPIC converter, at higher duty cycles is not an appropriate solution.

$$M_{CCM_{POSLLC}} = \frac{2-d}{1-d} \tag{1}$$



(a) (b)

Figure 1. POSLLC: (a) Circuit layout (b) M_{CCM} vs. duty cycle

Numerous approaches have been adopted in DC-DC converters to enhance the boosting capabilities, and extensive research has been conducted in this area. Mohammed and Alshamaa (2020) proposed a Luo converter that offers enhanced voltage gain over the POSLLC by substituting the single inductor in the POSLLC with a switched-capacitor-inductor cell. However, the voltage gain achieved in this modified converter remains low and requires further enhancement. Furthermore, Ramu et al. (2022) suggested another Luo converter, which offers a single input and multiple output step-up converter. The voltages at both outputs, however, remains insufficient and requires further enhancement. Other techniques of increasing the voltage gain and the output voltage include cascade (Vinnikov et al., 2012; Ortiz-Lopez et al., 2008), quadratic (Dizangian et al., 2025; Babaiahgari et al., 2025), interleaved (Algamluoli and Wu, 2023; Allehyani, 2023), and multilevel (Khalid et al., 2022; Shoaei et al., 2022) converters. In all these techniques, the voltage gain is high; nevertheless, the component count is also high, which will increase the losses and decrease efficiency. Several configurations of switched-inductor (SL) cells and switched-capacitor cells have been presented and discussed in Axelrod, Berkovich, and Ioinovici (2008). These cells play a crucial role in enhancing the voltage gain when they are integrated with conventional DC-DC converters either to step-up or step-down the input voltage.

The remainder of the article is structured as follows: Sections 2, 3, and 4 detail the proposed topologies (topology 1, topology 2, and topology 3), outlining the two primary modes of operation, along with a detailed derivation of the voltage gain and voltage stress across the semiconductor switches. In Section 5, a comparison is made between the three proposed topologies and various recent non-isolated step-up published converters, focusing on different aspects. Section 6 presents the simulation results, comparing them to the previously explained theoretical concepts. The concluding section is presented in section 7, summarizing the entire paper.

2. TOPOLOGY-I

2.1. Power Circuit

Topology-I is derived from the conventional POSLLC circuit, which has been modified by replacing the single inductor with a switched-inductor (SL) cell, as illustrated in Figure 2(a). The SL cell employs two inductors and three diodes. The main objective of modifying the original POSLLC is to attain a greater voltage gain than the POSLLC.

The first topology consists of two inductors (L_1 and L_2), two capacitors (C_1 and C_0), five diodes (D_1, D_2, D_3, D_4, and D_5), and a single active switch (S). The arrangement of the first topology circuit is as illustrated in Figure 2(b). Furthermore, it involves two modes of operation: on mode and off mode.

2.2. Modes of Operation

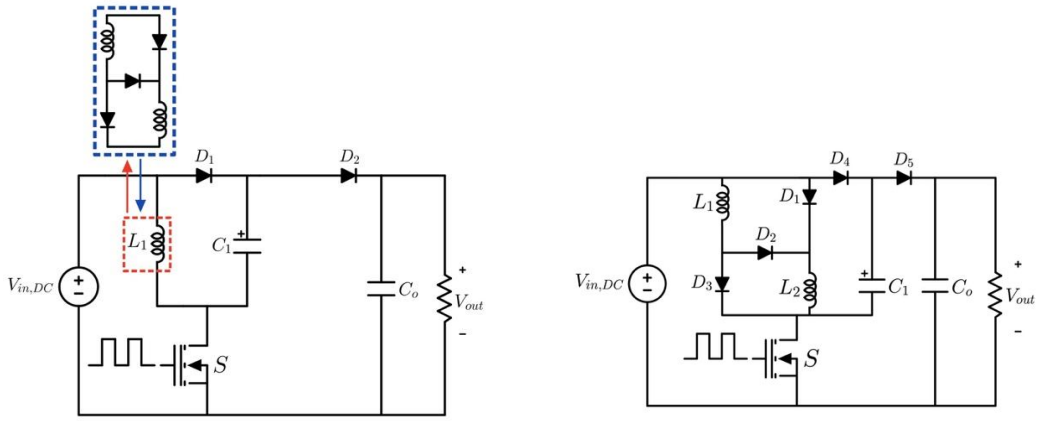
The following analysis of the proposed three topologies is based on the following assumptions: First, all circuit elements are considered lossless and 100% efficient. Second, the values of the inductors and capacitors are very large to keep the converter operation in continuous conduction mode (CCM) and to maintain constant voltage with zero ripple. The on mode occurs when S is on, which means it acts as a short circuit, as illustrated in Figure 3(a). In this mode of operation, D_2 and D_5 are reverse-biased, while L_1 and L_2 of the SL cell, along with C_1, are charged in parallel by the input voltage (V_{in}). Therefore, the voltage across L_1, L_2, and C_1 is expressed in equation (2). The output capacitor (C_0) supplies the load.

$$V_{L_1} = V_{L_2} = V_{C_1} = V_{in} \tag{2}$$

The off mode occurs when S is off, which means it acts as an open circuit, as illustrated in Figure 3(b). In this mode of operation, D_1, D_3, and D_4 are reverse-biased, while L_1 and L_2 of the SL cell and C_1 are discharged through the load. By applying Kirchhoff's Voltage Law (KVL) around the loop, equation (3) is obtained. Subsequently, equation (4) expresses the voltages across L_1 and L_2.

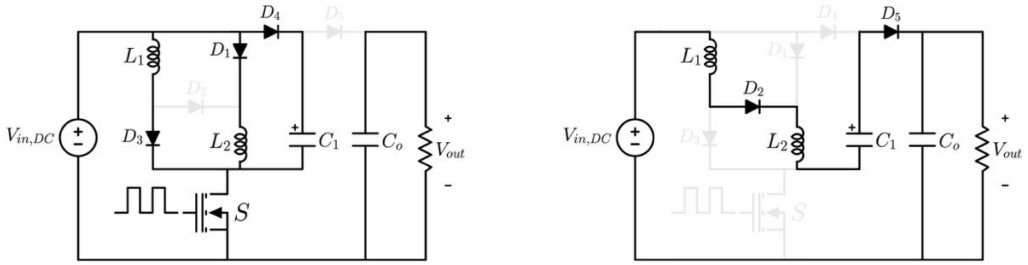
$$-V_{in} + V_{L_1} + V_{L_2} - V_{C_1} + V_{out} = 0 \tag{3}$$

$$V_{L_1} = V_{L_2} = \frac{2V_{in} - V_{out}}{2} \tag{4}$$



(a) (b)

Figure 2. Circuit layout of Topology-I with integrated SL cell: (a) derivation (b) main circuit



(a) (b)

Figure 3. Topology-I: (a) on mode (b) off mode

2.3. Voltage Gain and Voltage Stress Derivations

In steady state, the average voltage across the inductors is zero, which is an application of the volt-second balance principle. This principle is applied to equations (2) and (4), resulting in equation (5). Consequently, the CCM voltage gain for Topology-I (M_{CCM1}) is obtained, as shown in equation (6).

$$V_{in}d + \left(\frac{2V_{in} - V_{out}}{2}\right)(1-d) = 0 \tag{5}$$

$$M_{CCM_1} = \frac{V_{out}}{V_{in}} = \frac{I_{in}}{I_{out}} = \frac{2}{1-d} \tag{6}$$

The voltage stresses on either the diode or the switch indicate the diode or switch peak voltage during off mode. The equations for voltage stresses are derived from the equations for Topology-I mentioned above. Equations (7) and (8) refer to voltage stresses across diodes that are reverse-biased in the on mode.

$$V_{D_2} = V_{in} = \frac{(1-d)V_{out}}{2} \tag{7}$$

$$V_{D_5} = \frac{(1+d)V_{in}}{1-d} = \frac{(1+d)V_{out}}{2} \tag{8}$$

Equations (9) and (10) refer to voltage stresses across diodes and the switch that are reverse-biased or off in the off mode.

$$V_{D_1} = V_{D_3} = \frac{dV_{in}}{1-d} = \frac{dV_{out}}{2} \tag{9}$$

$$V_{D_4} = V_S = \frac{(1+d)V_{in}}{1-d} = \frac{(1+d)V_{out}}{2} \tag{10}$$

3. TOPOLOGY-II

3.1. Power Circuit

Topology-II is derived from Topology-I, which has been modified by replacing the two inductors with two SL cells as illustrated in Figure 4(a). Each SL cell utilizes two inductors and three diodes. The main objective of modifying the first topology is to attain a greater voltage gain than Topology-I.

The second topology consists of four inductors (L_1, L_2, L_3, and L_4), two capacitors (C_1 and C_0), eleven diodes (D_1, D_2, D_3, D_4, D_5, D_6, D_7, D_8, D_9, D_{10}, and D_{11}), and a single active switch (S). The arrangement of the second topology circuit is as illustrated in Figure 4(b). Furthermore, it involves two modes of operation: on mode and off mode.

3.2. Modes of Operation

The on mode occurs when S is on, as illustrated in Figure 5(a). In this mode of operation, D_2, D_5, D_8, and D_{11} are reverse-biased, while L_1, L_2, L_3, and L_4 of the SL cell, along with C_1, are charged in parallel by V_{in}. Therefore, the voltage across L_1, L_2, L_3, L_4, and C_1 is expressed in equation (11). C_0 supplies the load.

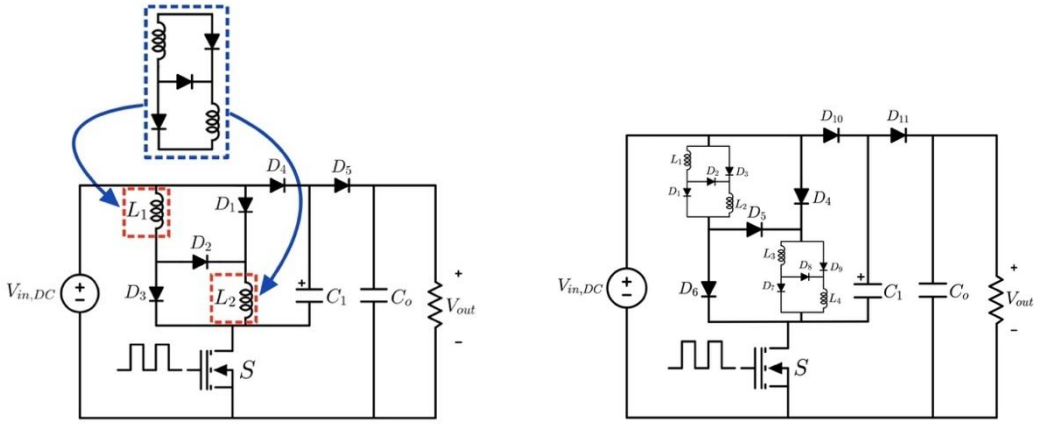
$$V_{L_1} = V_{L_2} = V_{L_3} = V_{L_4} = V_{C_1} = V_{in} \tag{11}$$

The off mode occurs when S is off, as illustrated in Figure 5(b). In this mode of operation, D_1, D_3, D_4, D_6, D_7, D_9, and D_{10} are reverse-biased, while L_1, L_2. L_3, and L_4 of the SL cell and C_1 are discharged

through the load. By applying KVL around the loop, equation (12) is obtained. Subsequently, equation (13) expresses the voltages across L_1, L_2, L_3, and L_4.

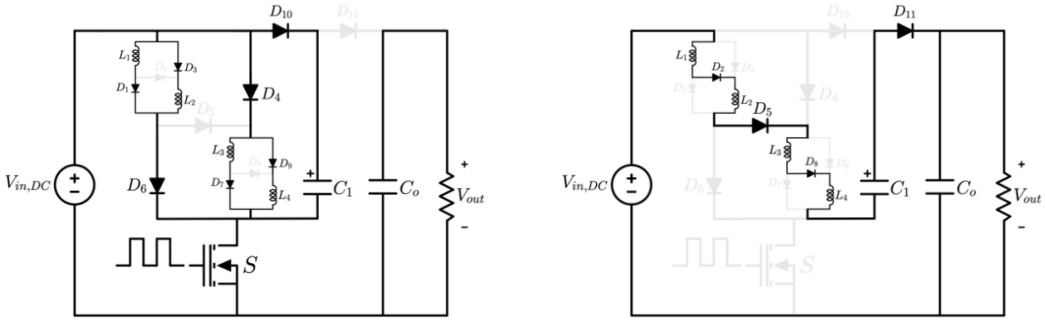
$$-V_{in} + V_{L_1} + V_{L_2} + V_{L_3} + V_{L_4} - V_{C_1} + V_{out} = 0 \tag{12}$$

$$V_{L_1} = V_{L_2} = V_{L_3} = V_{L_4} = \frac{2V_{in} - V_{out}}{4} \tag{13}$$



(a) (b)

Figure 4. Circuit layout of Topology-II with two integrated SL cells: (a) derivation (b) main circuit



(a) (b)

Figure 5. Topology-II: (a) on mode (b) off mode

3.3. Voltage Gain and Voltage Stress Derivations

The average inductor voltage is zero in steady state, which is an application of the volt-second balance principle. This principle is applied to equations (11) and (13), resulting in equation (14). Consequently, the CCM voltage gain for Topology-II (M_{CCM2}) is obtained, as shown in equation (15).

$$V_{in}d + \left(\frac{2V_{in} - V_{out}}{4}\right)(1 - d) = 0 \tag{14}$$

$$M_{CCM_2} = \frac{V_{out}}{V_{in}} = \frac{I_{in}}{I_{out}} = \frac{2(1 + d)}{1 - d} \tag{15}$$

The equations for voltage stresses are derived from the equations for Topology-II mentioned above. Equations (16) and (17) refer to voltage stresses across diodes that are reverse-biased in the on mode.

$$V_{D_2} = V_{D_5} = V_{D_8} = V_{in} = \frac{(1-d)V_{out}}{2(1+d)} \tag{16}$$

$$V_{D_{11}} = \frac{(1+3d)V_{in}}{1-d} = \frac{(1+3d)V_{out}}{2(1+d)} \tag{17}$$

Equations (18), (19), and (20) refer to voltage stresses across diodes and the switch that are reverse-biased or off in the off mode.

$$V_{D_1} = V_{D_3} = V_{D_7} = V_{D_9} = \frac{dV_{in}}{1-d} = \frac{dV_{out}}{2(1+d)} \tag{18}$$

$$V_{D_4} = V_{D_6} = \frac{2dV_{in}}{1-d} = \frac{dV_{out}}{1+d} \tag{19}$$

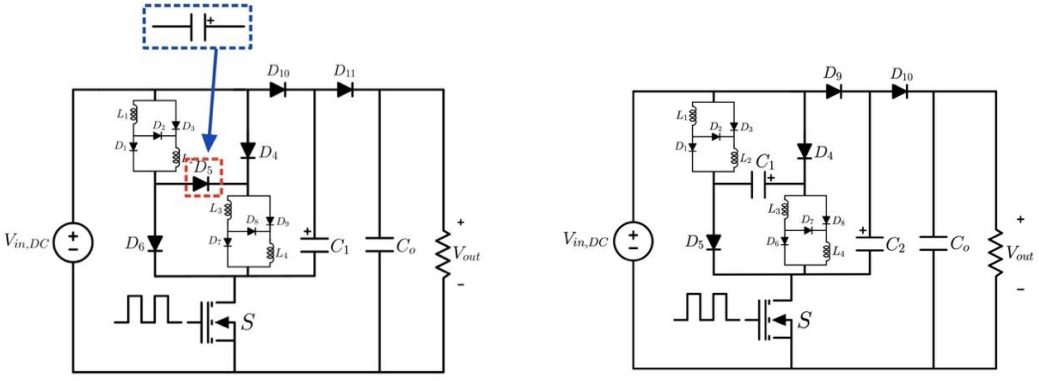
$$V_{D_{10}} = V_S = \frac{(1+3d)V_{in}}{1-d} = \frac{(1+3d)V_{out}}{2(1+d)} \tag{20}$$

4. TOPOLOGY-III

4.1. Power Circuit

Topology-III is derived from Topology-II, which has been modified by replacing diode D_2 with a capacitor, as illustrated in Figure 6(a). The main objective of modifying the second topology is to attain a greater voltage gain than Topology-II.

The third topology consists of four inductors (L_1, L_2, L_3, and L_4), three capacitors (C_1, C_2, and C_0), ten diodes (D_1, D_2, D_3, D_4, D_5, D_6, D_7, D_8, D_9, and D_{10}), and a single active switch (S). The arrangement of the third topology circuit is as illustrated in Figure 6(b). Furthermore, it involves two modes of operation: on mode and off mode.



(a) (b)

Figure 6. Circuit layout of Topology-III with D_2 in Topology-II swapped by capacitor: (a) derivation (b) main circuit

4.2. Modes of Operation

The on mode occurs when S is on, as illustrated in Figure 7(a). In this mode of operation, D_2, D_7, and D_{10} are reverse-biased, while L_1, L_2, L_3, and L_4 of the SL cell, along with C_1 and C_2, are charged in

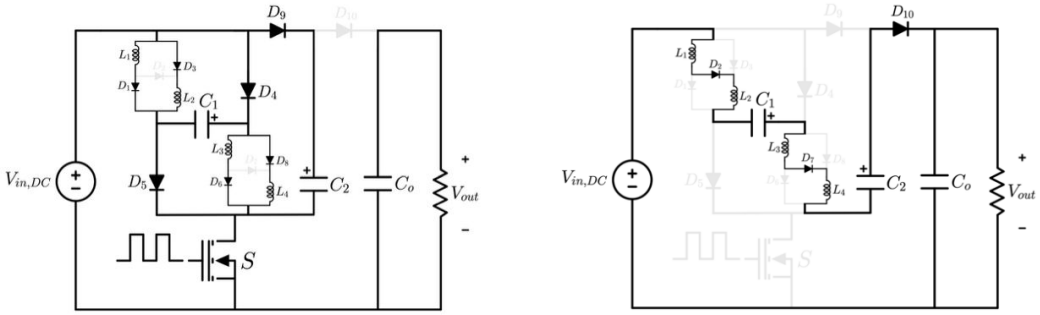
parallel by V_{in}. Therefore, the voltage across L_1, L_2, L_3, L_4, and C_1 is expressed in equation (21). C_0 supplies the load.

$$V_{L_1} = V_{L_2} = V_{L_3} = V_{L_4} = V_{C_1} = V_{C_2} = V_{in} \tag{21}$$

The off mode occurs when S is off, as illustrated in Figure 7(b). In this mode of operation, D_1, D_3, D_4, D_5, D_6, D_8, and D_9 are reverse-biased, while L_1, L_2. L_3, and L_4 of the SL cell and C_1 and C_2 are discharged through the load. By applying KVL around the loop, equation (22) is obtained. Subsequently, equation (23) expresses the voltages across L_1, L_2, L_3, and L_4.

$$-V_{in} + V_{L_1} + V_{L_2} + V_{L_3} + V_{L_4} - V_{C_1} - V_{C_2} + V_{out} = 0 \tag{22}$$

$$V_{L_1} = V_{L_2} = V_{L_3} = V_{L_4} = \frac{3V_{in} - V_{out}}{4} \tag{23}$$



(a) (b)

Figure 7. Topology-III: (a) on mode (b) off mode

4.3. Voltage Gain and Voltage Stress Derivations

The average inductor voltage across the inductors is zero in steady state, which is an application of the volt-second balance principle. This principle is applied to equations (21) and (23), resulting in equation (24). Consequently, the CCM voltage gain for Topology-III (M_{CCM3}) is obtained, as shown in equation (25).

$$V_{in}d + \left(\frac{3V_{in} - V_{out}}{4}\right)(1 - d) = 0 \tag{24}$$

$$M_{CCM_3} = \frac{V_{out}}{V_{in}} = \frac{I_{in}}{I_{out}} = \frac{3 + d}{1 - d} \tag{25}$$

The equations for voltage stresses are derived from the equations for Topology-III mentioned above. Equations (26) and (27) refer to voltage stresses across diodes that are reverse-biased in the on mode.

$$V_{D_2} = V_{D_7} = V_{in} = \frac{(1 - d)V_{out}}{3 + d} \tag{26}$$

$$V_{D_{10}} = \frac{2(1 + d)V_{in}}{1 - d} = \frac{2(1 + d)V_{out}}{3 + d} \tag{27}$$

Equations (28), (29), and (30) refer to voltage stresses across diodes or the switch that are reverse-biased or off in the off mode.

$$V_{D_1} = V_{D_3} = V_{D_6} = V_{D_8} = \frac{dV_{in}}{1-d} = \frac{dV_{out}}{3+d} \tag{28}$$

$$V_{D_4} = V_{D_5} = \frac{(1+d)V_{in}}{1-d} = \frac{(1+d)V_{out}}{3+d} \tag{29}$$

$$V_{D_9} = V_S = \frac{2(1+d)V_{in}}{1-d} = \frac{2(1+d)V_{out}}{3+d} \tag{30}$$

5. COMPARISON ANALYSIS

The suggested three modified Luo converters are evaluated against the boost converter, POSLLC, and four additional step-up converter topologies, as illustrated in Table 1. This comparison focuses on the voltage gain, voltage stress across the main active switch (S), and the component count required to construct each converter. The large main active switch voltage stress leads to higher overall costs for the converter and decreases its efficiency. Both the boost converter and the POSLLC require a small number of components to construct their circuit and can maintain a very low voltage gain of 4 and 5, respectively. Furthermore, the main active switch voltage stress of the boost converter is larger than its output voltage while the main active switch voltage stress of the POSLLC is lower than its output voltage. The step-up converters discussed in Chandrasekar and Lakshmanan (2025), Qin et al. (2021), Zhang et al. (2018) and Rafiee and Batmani (2025) achieve voltage gains of 6, 7, 9, and 12, respectively, when operating at a duty cycle of 0.75. However, the total circuit elements used in these converters is comparatively large, especially considering the low voltage gains they provide. Topology-I, Topology-II, and Topology-III achieve voltage gains of 8, 14, and 15, respectively, when operating at a duty cycle of 0.75. While these gains are relatively high, especially in Topology-II and Topology-III, they come at the cost of requiring more components to construct their converter circuits. Figure 8 clearly demonstrates the achievement of high voltage gain in comparison to the other converters. The step-up converter in Zhang, N. et al. (2018) achieves a higher voltage gain when operating at high duty cycles. Nevertheless, it is worth noting that operating the converter at extreme duty cycles is not recommended and results in many drawbacks, as mentioned earlier. Furthermore, the main active switch voltage stress of these four converters is greater than their output voltages. On the other hand, the main active switch voltage stress of the suggested topologies is less than their output voltages, which is another advantage besides their high voltage gain.

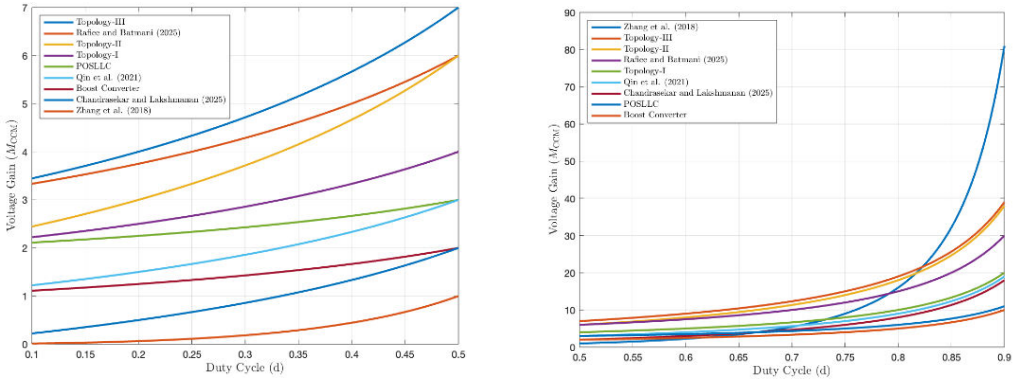
6. SIMULATION RESULTS

The design parameters for simulating Topology-I, Topology-II, and Topology-III are presented in Table 2. As shown in the table, the input voltage is 12 V, and the output voltages for the three topologies, Topology-I, Topology-II, and Topology-III, are 90 V, 150 V, and 160 V, respectively. Furthermore, the switching frequency utilized in these topologies is 50 kHz, and the duty cycle is 75%. Finally, the values of the four inductors and three capacitors used in the three topologies are 300 μH and 600 μF, respectively. The ideal output voltages of the proposed three topologies at an input voltage of 12 V and a duty cycle of 0.75 are calculated as 96 V, 168 V, and 180 V based on the derived gains in equations (6), (15), and (25), respectively. However, the simulated output voltages of Topology-I, Topology-II, and Topology-III are 90 V, 150 V, and 160 V, respectively. This inconsistency is due to the presence of non-ideal circuit elements in the simulation, such as diode forward voltage drops, switch on-state resistance, and parasitic elements of inductors and capacitors.

Table 1. Comparative analysis of the proposed topologies with previously proposed converters with respect to voltage gain, main switch voltage stress, and component count

Topology	M_{CCM}	M_{CCM} at d = 0.75	V_S	Component Count S/D/L/C/T
Boost Converter	$\frac{1}{1-d}$	4	Equals V_{out}	1/1/1/1/4
POSLLC	$\frac{2-d}{1-d}$	5	Less than V_{out}	1/2/1/2/6
Chandrasekar and Lakshmanan (2025)	$\frac{2d}{1-d}$	6	Equals V_{out}	1/6/2/4/13
Qin et al. (2021)	$\frac{1+d}{1-d}$	7	Larger than V_{out}	1/8/3/3/15
Zhang et al. (2018)	$\frac{d^2}{(1-d)^2}$	9	Larger than V_{out}	1/5/3/3/12
Rafiee and Batmani (2025)	$\frac{3}{1-d}$	12	Equals V_{out}	1/8/3/3/15
Topology-I	$\frac{2}{1-d}$	8	Less than V_{out}	1/5/2/2/10
Topology-II	$\frac{2(1+d)}{1-d}$	14	Less than V_{out}	1/11/4/2/18
Topology-III	$\frac{3+d}{1-d}$	15	Less than V_{out}	1/10/4/3/18

Note: M_{CCM} = voltage gain in continuous conduction mode (CCM), d = duty cycle, V_S = voltage stress across active switch, V_{out} = output voltage, S = no. of switches, D = no. of diodes, L = no. of inductors, C = no. of capacitors, T = total no. of components.



(a) (b)

Figure 8. M_{CCM} vs. *d* comparison (a) from 0.1 to 0.5 (b) from 0.5 to 0.9

Table 2. Design parameters of the proposed topologies

Parameter	Value
Input voltage (V_{in})	12 V
Output voltage (V_{out})	90 V, 150 V, 160 V
Output power (P_{out})	200 W
Switching frequency (f_s)	50 kHz
Duty cycle *(d)*	75%
Inductors (L_1, L_2, L_3, and L_4)	300 μH
Capacitors (C_1, C_2, and C_0)	600 μF

6.1. Topology-I

A 200 W, 90 V model was constructed and simulated in MATLAB/Simulink to evaluate the derived equations discussed in the theoretical section above for Topology-I. First, the output voltage is evaluated, as illustrated in Figure 9. The output voltage can be calculated from equation (6), which is the voltage gain of Topology-I in CCM. The calculated value is 96 V under ideal conditions, whereas the lower value observed in Figure 9 reflects simulation results that include non-ideal effects. Then, the voltage stresses across all the switches in Topology-I were evaluated in both the on mode and the off mode, as illustrated in Figure 10 and Figure 11, respectively. In the on mode, two diodes are reverse biased: D_2 and D_5. Their voltage stress can be calculated using equations (7) and (8). The calculated values are $V_{D2} = 11$ V and $V_{D5} = 78$ V, which shows good agreement with the data presented in Figure 10. In the off mode, three diodes (D_1, D_3, and D_4) are reverse biased, and the active switch (S) is off. Their voltage stress can be calculated using equations (9) and (10). The calculated values are $V_{D1} = V_{D3} = 34$ V and $V_{D4} = V_S = 78$ V, which shows good agreement with the data presented in Figure 11.

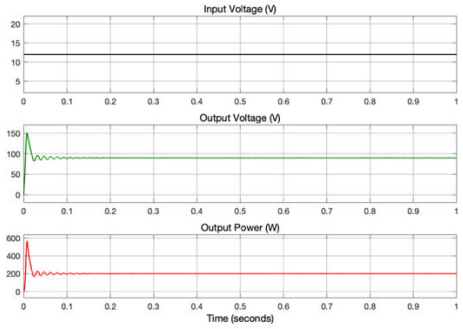
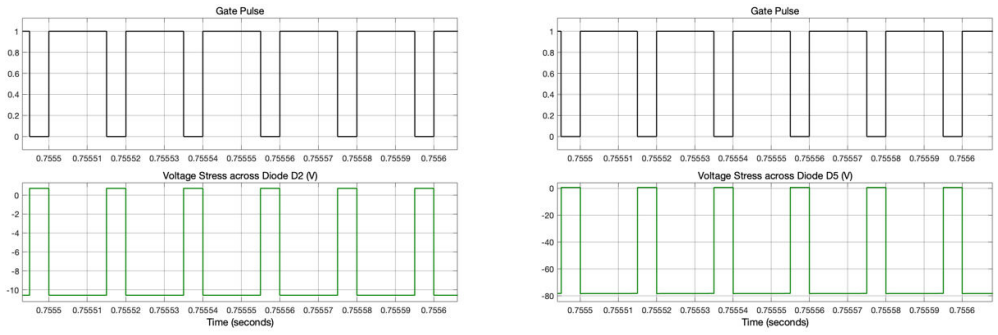
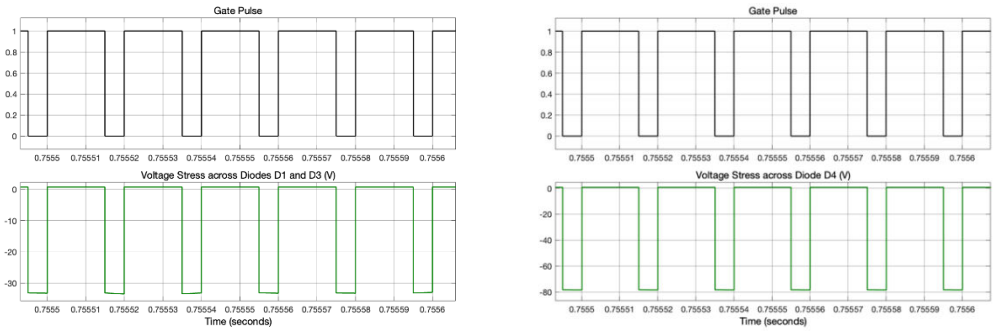


Figure 9. V_{in}, V_{out}, and P_{out} of Topology-I



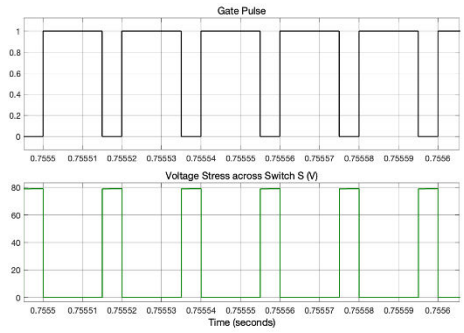
(a) (b)

Figure 10. Voltage stress of Topology-I in on mode: (a) across D_2 (b) across D_5



(a)

(b)



(c)

Figure 11. Voltage stress of Topology-I in off mode: (a) across D_1 and D_3 (b) across D_4 (c) across S

6.2. Topology-II

A 200 W, 150 V model was constructed and simulated in MATLAB/Simulink to evaluate the derived equations discussed in the theoretical section above for Topology-II. First, the output voltage is evaluated, as illustrated in Figure 12. The output voltage can be calculated from equation (15), which is the voltage gain of Topology-II in CCM. The calculated value is 168 V under ideal conditions, whereas the lower value observed in Figure 12 reflects simulation results that include non-ideal effects. Then, the voltage stresses across all the switches in Topology-II were evaluated in both the on mode and the off mode, as illustrated in Figure 13 and Figure 14, respectively. In the on mode, four diodes are reverse biased: D_2, D_5, D_8, and D_{11}. Their voltage stress can be calculated using equations (16) and (17). The calculated values are $V_{D2} = V_{D5} = V_{D8} = 11$ V and $V_{D11} = 137$ V, which shows good agreement with the data presented in Figure 13. In the off mode, seven diodes (D_1, D_3, D_4, D_6, D_7, D_9, and D_{10}) are reverse biased, and the active switch (S) is off. Their voltage stress can be calculated using equations (18), (19), and (20). The calculated values are $V_{D1} = V_{D3} = V_{D7} = V_{D9} = 32$ V, $V_{D4} = V_{D6} = 63$ V, and $V_{D10} = V_S = 137$ V, which shows good agreement with the data presented in Figure 14.

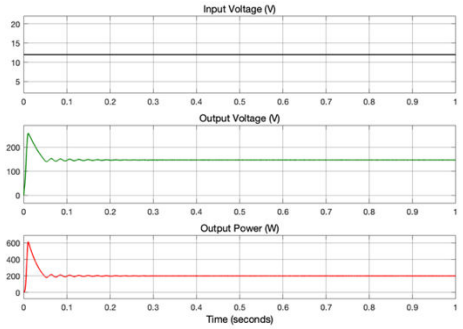
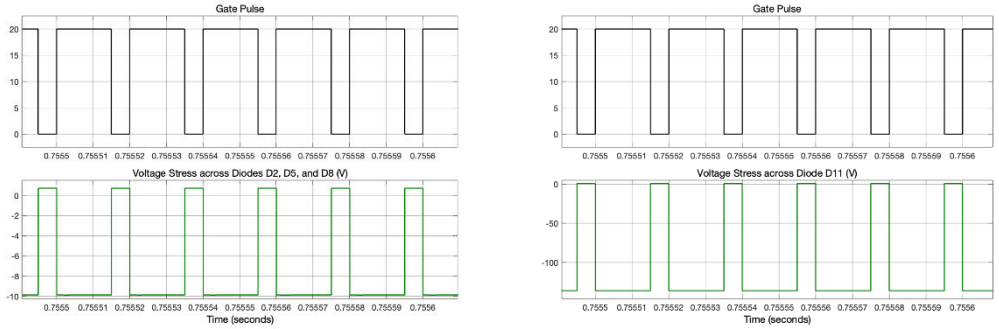
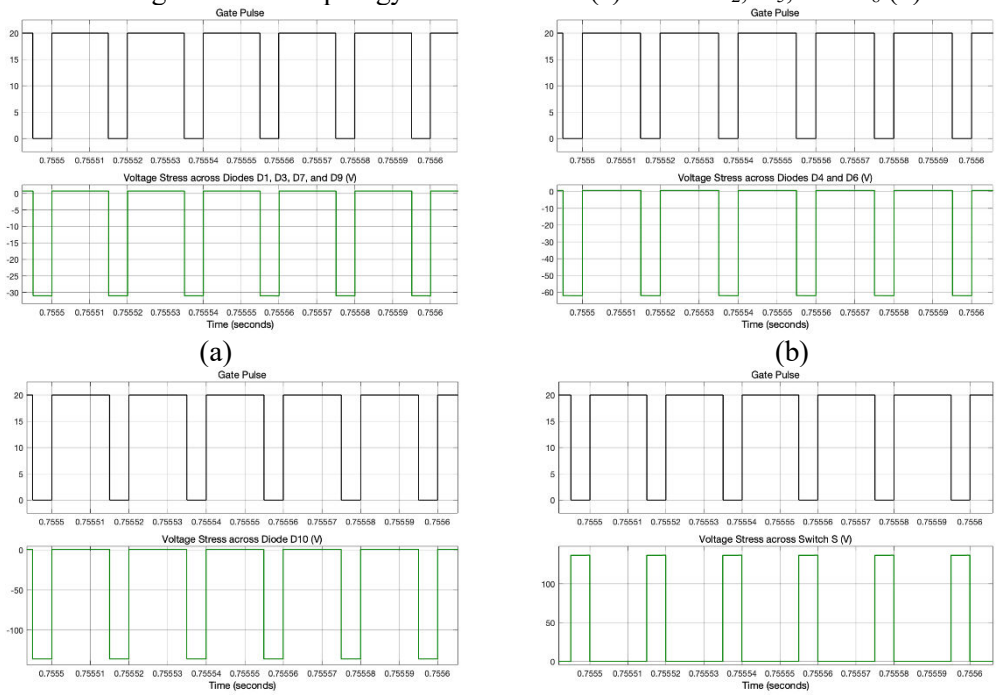


Figure 12. V_{in}, V_{out}, and P_{out} of Topology-II



(a) (b)

Figure 13. Voltage stress of Topology-II in on mode: (a) across D_2, D_5, and D_8 (b) across D_{11}



(a) (b)

(c) (d)

Figure 14. Voltage stress of Topology-II in off mode: (a) across D_1, D_3, D_7, and D_9 (b) across D_4 and D_6 (c) across D_{10} (d) across S

6.3. Topology-III

A 200 W, 160 V model was constructed and simulated in MATLAB/Simulink to evaluate the derived equations discussed in the theoretical section above for Topology-III. First, the output voltage is evaluated, as illustrated in Figure 15. The output voltage can be calculated from equation (25), which is the voltage gain of Topology-III in CCM. The calculated value is 180 V under ideal conditions, whereas the lower value observed in Figure 15 reflects simulation results that include non-ideal effects. Then, the voltage stresses across all the switches in Topology-III were evaluated in both the on mode and the off mode, as illustrated in Figure 16 and Figure 17, respectively. In the on mode, three diodes are reverse biased: D_2, D_7, and D_{10}. Their voltage stress can be calculated using equations (26) and (27). The calculated values are $V_{D2} = V_{D7} = 11$ V and $V_{D10} = 148$ V, which shows good agreement with the data presented in Figure 16. In the off mode, seven diodes (D_1, D_3, D_4, D_5, D_6, D_8, and D_9) are reverse biased, and the active switch (S) is off. Their voltage stress can be calculated using equations (28), (29), and (30). The calculated values are $V_{D1} = V_{D3} = V_{D6} = V_{D8} = 32$ V, $V_{D4} = V_{D5} = 74$ V, and $V_{D9} = V_S = 147$ V, which shows good agreement with the data presented in Figure 17.

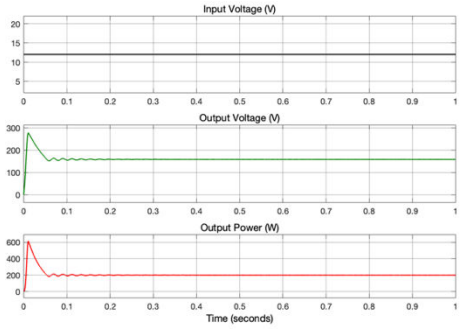
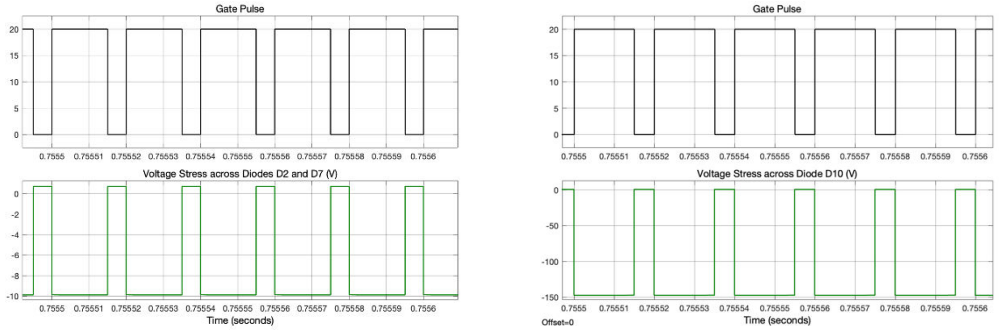
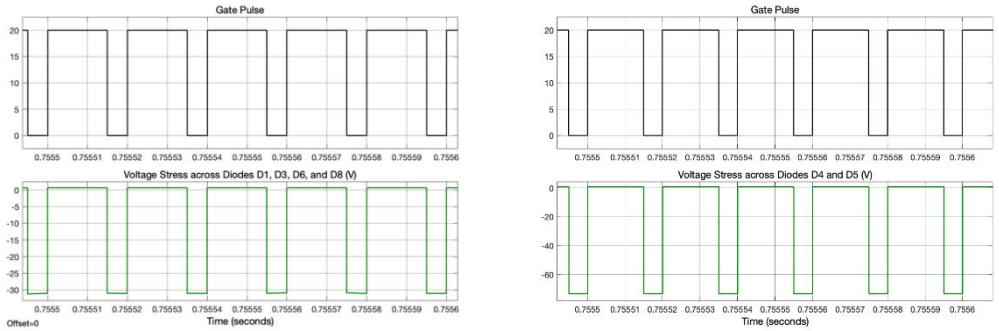


Figure 15. V_{in}, V_{out}, and P_{out} of Topology-III

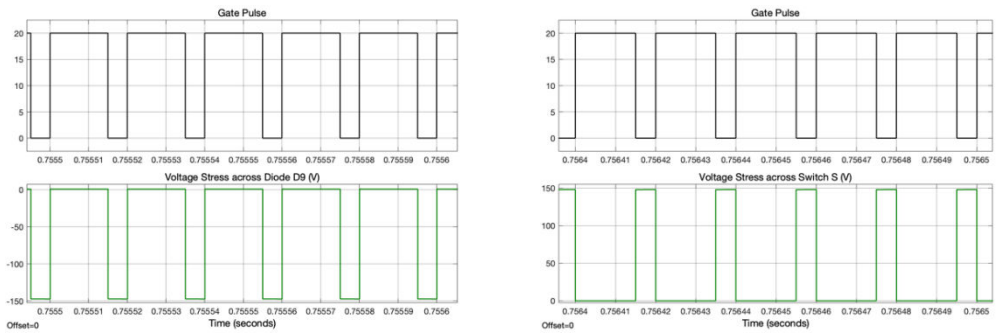


(a) (b)

Figure 16. Voltage stress of Topology-III in on mode: (a) across D_2 and D_7 (b) across D_{10}



(a) (b)



(c) (d)

Figure 17. Voltage stress of Topology-III in off mode: (a) across D_1, D_3, D_6, and D_8 (b) across D_4 and D_5 (c) across D_9 (d) across S

6.4. Input Voltage Disturbance

A disturbance is introduced to the input voltage in order to assess the stability of the three proposed topologies. This disturbance involves a change in the input voltage, increasing from 12 V to 18 V, which is a 50% increase, and then returning to 12 V. The proposed three topologies remain stable after the sudden increase and decrease in the input voltage, as illustrated in Figure 18.

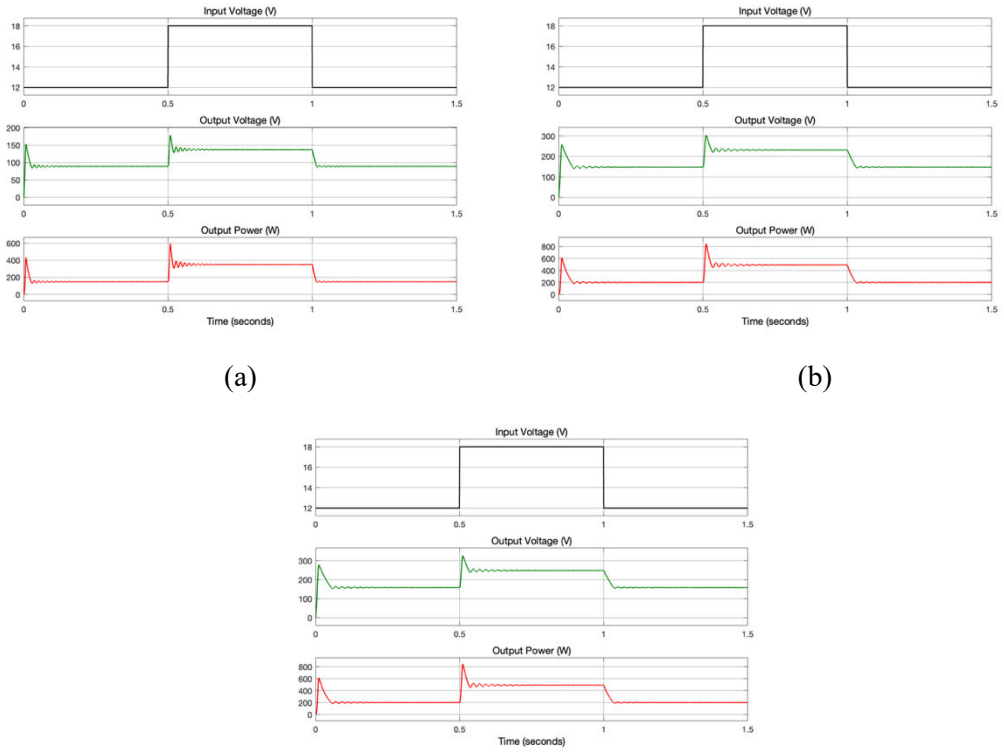


Figure 18. V_{out} and P_{out} responses to variations in V_{in}: (a) Topology-I (b) Topology-II (c) Topology-III

7. CONCLUSION

In this paper, three topologies—Topology-I, Topology-II, and Topology-III—are presented and discussed. They can significantly boost the input voltage without the need for coupled inductors or using extreme duty cycle values, simply by incorporating a few SL cells. Such converters with high voltage gain are critical in PV systems because of their ability to increase the low voltage generated by the PV. Topology-I is obtained by incorporating a single SL cell in place of an inductor in the POSLLC circuit. In contrast, Topology-II is developed by integrating two SL cells instead of two inductors found in Topology-I. Topology-III, however, is created by replacing diode D_2 in Topology-II with a capacitor to further enhance the voltage gain. Topology-I, Topology-II, and Topology-III accomplish voltage gains of 8, 14, and 15, respectively, when operating at a duty cycle of 0.75. However, the conventional POSLLC attains a voltage gain of only 5 when operating at a duty cycle of 0.75. The equations for the output voltage, along with the voltage stress on the switches, are derived and compared to the results obtained using MATLAB/Simulink software, and the results show good agreement.

Nomenclature

Nomenclature	
C	Capacitor
CCM	Continuous conduction mode
d	duty cycle
D	Diode
f_s	Switching frequency [Hz]
KVL	Kirchoff's Voltage Law
L	Inductor
M	Voltage gain
$POSLLC$	Positive output super lift Luo converter
P_{out}	Output power [W]
PV	Photovoltaic
R	Load resistor [Ω]
S	Switch
SL	Switched-inductor
V	Voltage [V]
V_{in}	Input voltage [V]
V_{out}	Output voltage [V]

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