

Novel Topology of Buck-Boost Switched-capacitor DC-DC Converter

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Submitted 24/02/2026, Accepted 05/05/2026, Available online 05/10/2026, Published 31/12/2026

DOI: [10.64518/uohjs.2026.07](https://doi.org/10.64518/uohjs.2026.07)

Abstract:

This paper introduces a new topology for a buck-boost switched-capacitor DC-DC converter. The inductorless design is achieved by combining the boost and buck series-parallel switched-capacitor converter topologies. The converter is composed of nine switches and three capacitors, two designated for charge-transfer and one serving as a filter capacitor. This innovative configuration enables efficient voltage step-up and step-down operations, offering a cost-effective, compact, and lightweight solution for DC-DC conversion. A control algorithm is used to control the switches, enabling seamless transitions between buck and boost modes. Following a brief introduction to switched-capacitor (SC) converters, the operational principles and mathematical modeling of the proposed converter are thoroughly discussed for each mode of operation. Additionally, simulation results are presented to assess the performance of the new buck-boost switched-capacitor DC-DC converter topology. The converter's functionality is evaluated under both loaded and no-load conditions.

Key words: DC-DC converters; buck-boost bonverter; switched capacitor (SC), boost converter, buck converter.

1. INTRODUCTION

DC-DC converters play a crucial role in power electronics due to their integration with various fields, including control systems, power systems, analog circuits, and electronic circuits (Axelrod et al., 2008). This paper introduces a novel topology for a DC-DC buck-boost converter designed for low-power applications, such as IC circuits. DC-DC converters are typically classified into two main categories: isolated and non-isolated converters, with each category further subdivided into different types.

Non-isolated converters are classified into two categories, inductor-based such as the conventional buck and boost converters, and capacitor-based such as switching-capacitor converters. The inductor-based converters emerged in the 1960s after the invention of the electronic switches known as transistors. They are considered to be the first DC-DC converters that use electronic switches to change the voltage from one level to another (Chander et al., 2010). Usually, they are used for high-power applications such as maximum power point tracker (MPPT) for renewable energy applications (Sharma et al., 2023). However, inductor-based converters cannot be used for low-power applications because of the presence of an inductor which creates challenges in implementing such converters on VLSI chips (Singh and Gupta, 2018). Those challenges are physical such as the large scale of the inductor size and substrate's poor insulation, and functional challenges due to the inductor emissions,

which can cause electromagnetic interference with other on-chip signals. Because of those difficulties and due to the high demand on VLSI technology, the first actual DC-DC switching-capacitor converter was developed in 1990 by (Umeno et al., 1991). This converter was an improvement for the switched-capacitor DC-DC charge pump converter which is first introduced in 1974 (Dickson, 1976). After this discovery, researchers and scientists from all over the world started to develop different topologies for switching-capacitor DC-DC converters such as step-up and step-down converter presented in reference (Makowski and Maksimovic, 1995).

This paper proposes a new topology for a switched-capacitor DC-DC converter, continuing on previous advancements aimed at enhancing IC circuit technology (Alateeq and Kalkur, 2017). This new topology has been analyzed and simulated to test its performance with different parameters. The modulation approach chosen for this work is Seeman's approach presented in reference (Seeman and Sanders, 2008), which is explained in detail in the following sections. The simulation software used throughout this project was the MATLAB Simulink software.

Most DC-DC converters based on the switched-capacitor approach are typically designed as either step-up or step-down configurations (Chung et al., 2000). Currently, only a few switched-capacitor topologies are capable of both stepping up and stepping down the input voltage, as is possible with the conventional buck-boost converter. To address this limitation, this work proposes a novel topology of switched capacitor DC-DC converter able to both step-up and step-down the voltage, continuing on previous advancements aimed at enhancing IC circuit technology. One of the few existing SC topologies capable of both step-up and step-down the voltage is the one presented in reference (Abraham et al., 2014). It introduces a multi-gain switched-capacitor converter capable of producing five discrete voltage conversion ratios. The circuit consists of two charge-transfer capacitors and eleven switches controlled by three distinct phases: ON-charging, ON-discharging, and OFF. Each switch requires a manual selection of the appropriate phase to achieve a certain voltage conversion ratio. Therefore, every switch must be individually adjusted for each conversion mode according to the switching sequence table provided in the paper (Abraham et al., 2014). This makes the control of the switches very complicated. On the other hand, the topology proposed in this work has two charge-transfer capacitors and only nine non-ideal switches, which reduces switching losses by using fewer active devices. The switches in this topology are divided into two groups, each controlled by a pulse signal that is complementary to the other, which enables two-phase control. Also, an algorithm is presented in this work to manage the dynamic switching between buck and boost modes. The proposed control algorithm operates by continuously comparing the input voltage with a reference voltage. The converter switches to boost mode when the comparison result is positive, otherwise, it switches to buck mode. This self-adaptive strategy removes the need for manual switch configuration and enables real-time regulation of the output voltage.

Table 1. Comparison Between the Proposed Converter and Abraham Topology

	Abraham Topology	Topology in This Work
Number of Phases	3 phases	2 phases
Number of Switches	11 Switches	Only 9 Switches
Control Complexity	No algorithm is proposed for control purposes	An algorithm is proposed for control purposes

2. THE BUCK-BOOST CONVERTER DESIGN

The aim of this paper is to introduce a novel inductorless buck-boost switched-capacitor converter. This new topology can be achieved by combining two different DC-DC converter topologies which are the series-parallel step-up and step-down presented in reference (Makowski and Maksimovic, 1995). To design the buck-boost converter, first, it is necessary to analyze the operation principle and the dynamic behavior of those two converters and their conversion ratios.

Both buck and boost converters have two different topologies for charging and discharging modes. This transformation between modes can be achieved by a set of switches controlled by two complementary pulse signals, Phase 1 and Phase 2 as shown in Figure 1.

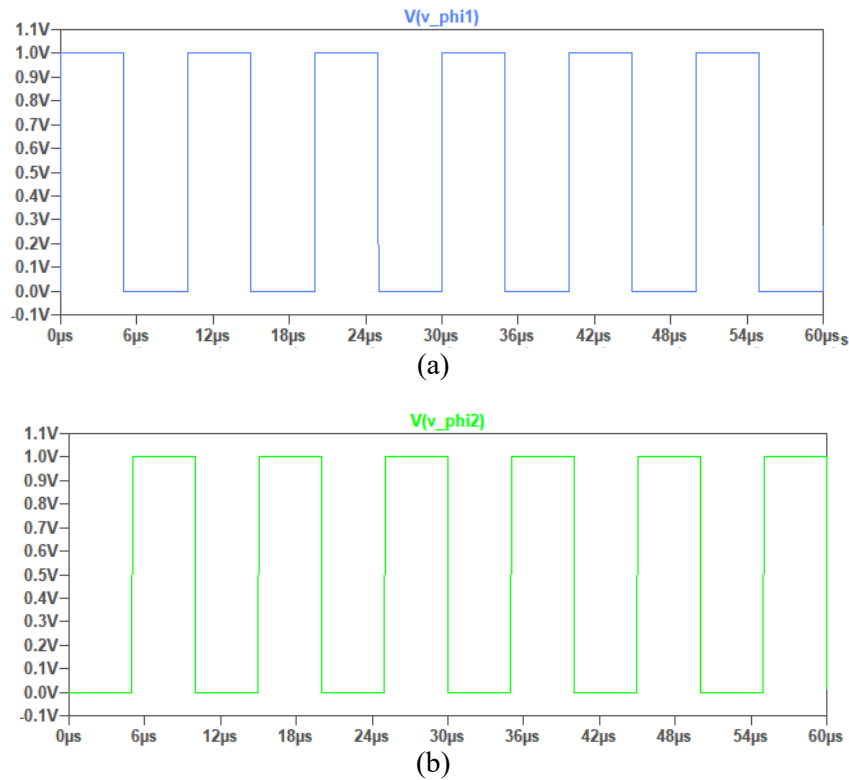


Figure 1. Pulse signals (a) phase 1, (b) Phase 2.

For series-parallel buck converter topology, as presented in Figure 2, it has a total of three capacitors and one resistor. The capacitors C_1 and C_2 are considered to be the charge transferring capacitors and C_L is the filter capacitor which is connected in parallel with the load. During phase 1, C_1 and C_2 are connected in parallel which forms a combination that is connected in series with the voltage source and the load C_L . During Phase 2, the voltage source is disconnected from the rest of the circuit so that C_1 and C_2 are connected in series and the whole combination is connected in parallel with C_L (Vilela et al., 1996).

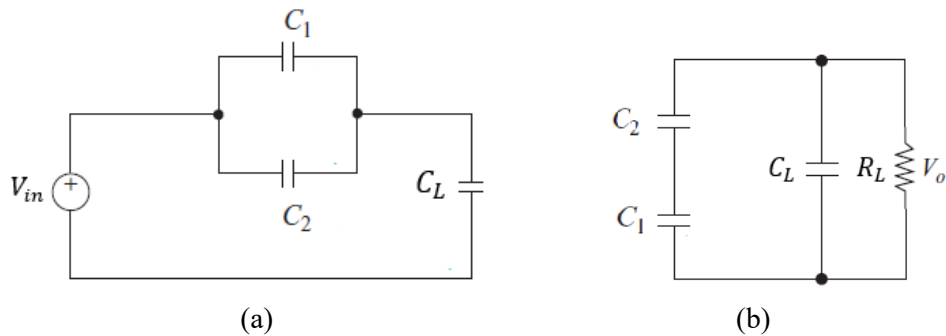


Figure 2. Series and parallel buck converter during (a) phase 1, (b) Phase 2

For series-parallel boost converter, as presented in Figure 3, during phase 1, the charge-transfer capacitors C_1 and C_2 are connected in parallel with the source and charged with V_s . During Phase 2, those charged capacitors C_1 and C_2 are connected in series and this combination of capacitors is connected in parallel with load capacitor C_L .

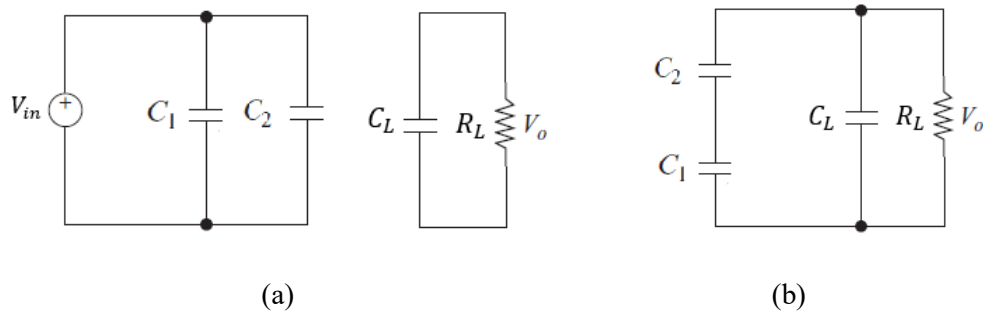


Figure 3. Series and parallel topology of boost converter during (a) phase 1, (b) Phase 2

The design of buck-boost converter can be achieved by combining the two topologies of buck and boost converters together. The challenge is that both of them are formed by two different topologies which means that four topologies have to be utilized in one circuit to design buck-boost converter. It can be seen from Figure 2 and Figure 3 that boost and buck converters share the same topology during Phase 2, in which C_1 and C_2 are connected in series and the whole combination is connected in parallel with the filter capacitor C_L . This feature brings us closer to the design of the buck-boost converter since the topologies during Phase 2 for both buck and boost converters are the same. Yet, the converter during Phase 1 must have the ability to switch from buck topology Figure 2 to boost topology Figure 3, in order to design buck-boost converter. This transformation between buck and boost topologies is possible by adding switches between the combination of the capacitors (C_1, C_2) and the filter capacitor C_L . Those switches are able to connect the combination of the transfer capacitors (C_1, C_2) with the filter capacitor C_L to form buck converter. Furthermore, they are able to connect the combination of the transfer capacitors (C_1, C_2) with the ground which will make the charge-transfer capacitors have a parallel connection with source which form the topology of boost converter during phase 1. To utilize this connection, two switches need to be added as in Figure 4.

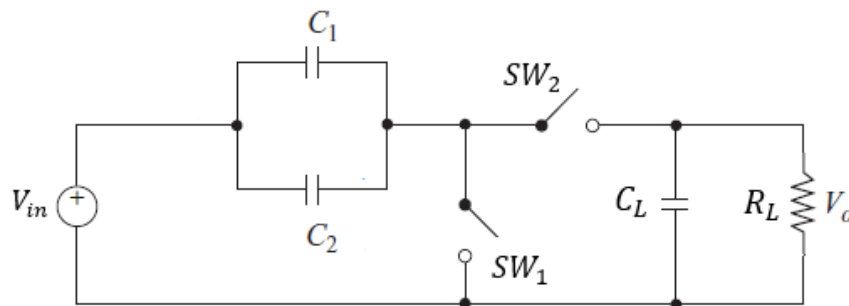


Figure 4. The extra switches that control the transition from buck to boost

For the buck converter, SW1 has to be off all the time to disconnect the ground for the rest of the circuit, and SW2 has to be ON all the time to connect the charge-transfer capacitors (C_1, C_2) with the filter capacitor C_L during Phase 1 and Phase 2. On the other hand, for boost converter SW1 has to be controlled by the pulse signal named Phase 1 to connect the charge-transfer capacitors (C_1, C_2) with the ground during Phase 1 which will make those capacitors connected in parallel with source and OFF during Phase 2. SW2 has to be controlled by the pulse signal named Phase 2 to control the connection between the charged capacitors (C_1, C_2) with load capacitor C_L during Phase 2 and OFF during phase 1.

3. CONVERTER ANALYSIS

3.1 Converter Analysis under No-load Conditions

The proposed buck-boost converter is capable of stepping up and stepping down the input voltage to a certain output voltage level by enabling and disabling specific switches (Wang et al., 2008). As mentioned earlier, both converters have the same topology during Phase 2 but different topologies during Phase 1. For boost converter, SC converter is able to step-up the input voltage to twice its value, which makes the conversion ratio is 2 by controlling switches SW1 and SW2, as in Figure 4. During the charging mode in phase 1, SW1 is controlled by the pulse signal phase 1, while SW2 is controlled by the pulse signal Phase 2. On the other hand, for buck converter, the conversion ratio is $2/3V_{in}$ which is achieved by keeping SW1 OFF all the time and SW2 ON all the time during phase 1.

The mathematical expression for the converter's conversion ratio can be realized by applying KVL for buck and boost converters during Phase 1 and Phase 2.

For the buck converter, voltage across C_1 and C_2 can be calculated by applying KVL to the circuit in Figure 2(a) during Phase 1 as follows:

$$V_{C1} = V_{C2} = V_{in} - V_0 \quad (1)$$

During Phase 2, voltage across C_1 and C_2 adds up by connecting those capacitors in series and all of them are connected in parallel with C_L . By applying KVL to this topology during phase 1, output voltage can be calculated as given in (2).

$$V_0 = V_{C1} + V_{C2} \quad (2)$$

The voltage conversion ratio gain of buck converter can be calculated by substituting Eq. (1) into Eq. (2) as follows:

$$V_0 = (V_{in} - V_0) + (V_{in} - V_0) \quad (3)$$

$$\frac{V_0}{V_{in}} = \frac{2}{3} \quad (4)$$

Eq. (4) shows that VCR for buck-boost converter during the buck mode is $2/3V_{in}$. For boost converter, voltage across C_1 and C_2 can be calculated by applying KVL to the circuit in Figure 3 during Phase 1 as given in Eq. (5)

$$V_{in} = V_{C1} = V_{C2} \quad (5)$$

During Phase 2, voltage across C_1 and C_2 adds up by connecting those capacitors in series and all of them are connected in parallel with C_L . By applying KVL to this topology during phase 2, output voltage can be calculated as presented in Eq. (6).

$$V_0 = V_{C1} + V_{C2} \quad (6)$$

The voltage conversion ratio gain of the boost converter can be calculated by substituting Eq. (5) into Eq. (6) as presented in Eq. (7).

$$V_0 = V_{in} + V_{in} \quad (7)$$

$$\frac{V_0}{V_{in}} = 2 \quad (8)$$

Eq. (8) shows that VCR for buck boost converter during the boost mode is double. For the case of no load, the buck-boost converter conversion ratio is $2V_{in}$ during the boost mode and $2/3V_{in}$ during the buck mode.

3.2 Converter Analysis under Loaded Conditions

The converter achieves an ideal conversion ratio under no-load conditions. In boost mode, the ideal output voltage of the converter is $2V_{in}$, while the ideal output voltage for buck mode is $2/3V_{in}$. However, this ideal conversion ratio is altered when a load is connected to the converter (Kumar et al., 2024). This ideal voltage is divided using voltage-divider rule between R_L and R_{loss} which represent the converter's switching loss and charging-discharging loss as in Figure 5.

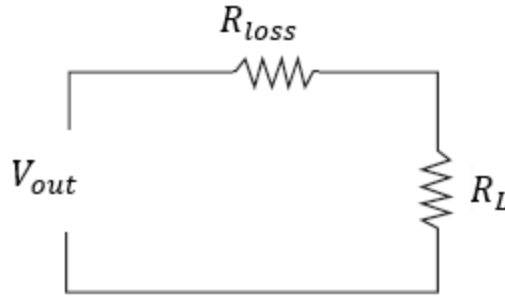
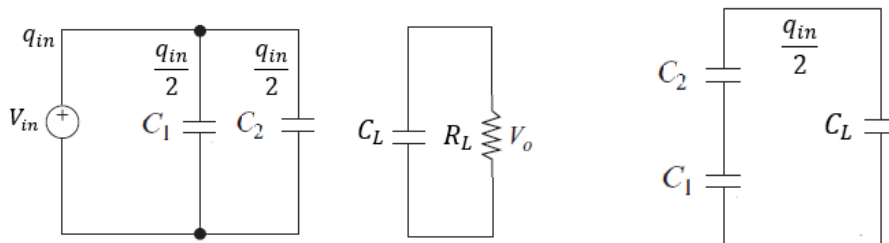


Figure 5. Actual converter output voltage across R_L

The converter loss resistance R_{loss} is a function of charge multiplier which has to be determined separately for buck mode and boost mode. In the switched-capacitor converter design, there are two phases, and each phase has a corresponding charge multiplier vector. Every capacitor or independent voltage source has a charge multiplier, which is defined as the amount of charge transferred through a specific element during one phase divided by the total output charge. The total output charge is the sum of the charges from both phase one and phase two.

To determine the converter's charge multiplier during boost mode, a circuit analysis must be performed for both phases. During phase 1, capacitors C_1 and C_2 are connected in parallel with V_{in} , and disconnected from C_L as in shown in Figure 6. By applying Kirchhoff's Current Law (KCL), the charge provided by the source is evenly split between the two capacitors, with each capacitor receiving a charge of $q_{in}/2$, assuming the capacitors are of equal size.



(a)

(b)

Figure 6. Charges distribution during boost mode for (a) Phase 1 (b) phase 2

Charge multiplier for boost mode during Phase 1 is as presented in Eq. (9)

$$a_1 = \left[\frac{q_{in}}{2} \quad \frac{q_{in}}{2} \right] / Q_{total} \quad (9)$$

During Phase 2, capacitors C_1 and C_2 are connected in series, and the entire combination is connected in parallel with the load capacitor C_L . The charges delivered to the load is $q_{in}/2$ which is the initial charge stored in the charge-transfer capacitors C_1 and C_2 during phase 1.

The total output charges is as presented in Eq. (10-12)

$$Q_{total} = q_{out1} + q_{out2} \quad (10)$$

$$= 0 + q_{in} \frac{1}{2} \quad (11)$$

$$= q_{in} \frac{1}{2} \quad (12)$$

Substituting the total output charges back to charge multiplier Eq. (9), yields the expressions presented in Eq. (13) and Eq. (14).

$$a_1 = \left[\frac{q_{in}}{2} \quad \frac{q_{in}}{2} \right] / q_{in} \frac{1}{2} \quad (13)$$

$$a_1 = a_2 = 1 \quad (14)$$

The loss resistance R_{Loss} is calculated by substituting the computed charge multipliers into Tellegen's theorem, which states that the total addition of all the charges through capacitor charges multiplied by their voltages should be zero. Applying this principle on the converter yields as follows:

$$v_{out} q_{out} + \sum q_i \Delta v_i = 0 \quad (15)$$

$$\Delta v_i = \frac{q_i}{c_i} \quad (16)$$

Substituting (16) into (15), and dividing by q_{out}^2 , yields as presented in Eq. (17-20).

$$\frac{v_{out}}{q_{out}} + \sum \frac{q_i * \frac{q_i}{c_i}}{q_{out}^2} = 0 \quad (17)$$

$$\frac{v_{out}}{q_{out}} + \sum \frac{1}{c_i} * \frac{q_i^2}{q_{out}^2} = 0 \quad (18)$$

$$\frac{v_{out}}{q_{out}} + \sum \frac{1}{c_i} * a_{ci}^2 = 0 \quad (19)$$

$$R_{loss} = \frac{v_{out}}{q_{out}} = \sum \frac{1}{c_i} * a_{ci}^2 \quad (20)$$

R_{loss} for the boost mode can be computed as given in Eq. (21).

$$R_{loss} = \frac{1}{F_{sw}} \left(\frac{1}{C1} + \frac{1}{C2} \right) \quad (21)$$

The same approach is going to be applied for buck mode. During phase 1, the charge-transfer capacitors C_1 and C_2 are connected in parallel, and the entire combination is connected in series with the voltage source and load capacitor C_L . The charge supplied by the source is evenly distributed between the two capacitors, with each capacitor receiving a charge of $q_{in}/2$, under the assumption that the capacitors are of equal size.

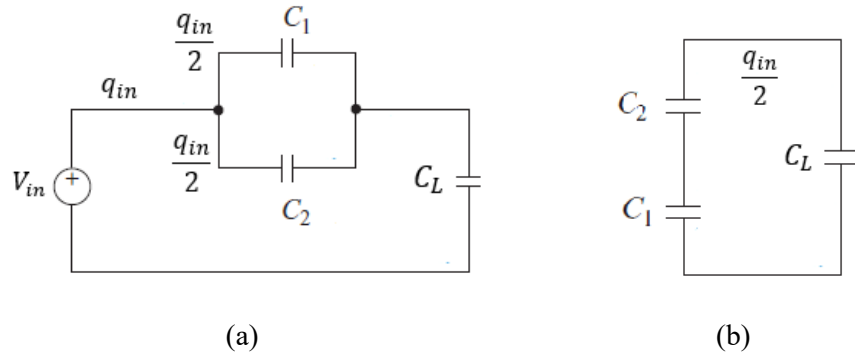


Figure 7. Charges distribution during buck mode for (a) Phase 1 (b) phase 2

Charge multiplier for buck mode during Phase 1 is as presented in Eq. (22).

$$a_1 = \left[\frac{q_{in}}{2} \quad \frac{q_{in}}{2} \right] / Q_{total} \quad (22)$$

During Phase 2, capacitors C_1 and C_2 are connected in series, and their combined configuration is connected in parallel with the load capacitor C_L , so that the charge delivered to the load is equal $q_{in}/2$. The total output charges is as given in Eq. (23-25).

$$Q_{total} = q_{out1} + q_{out2} \quad (23)$$

$$= 1 + q_{in} \frac{1}{2} \quad (24)$$

$$= q_{in} \frac{3}{2} \quad (25)$$

Substituting the total output charges back to charge multiplier in Eq. (22), yield to as presented in Eq. (26-27).

$$a_1 = \left[\frac{q_{in}}{2} \quad \frac{q_{in}}{2} \right] / q_{in} \frac{3}{2} \quad (26)$$

$$a_1 = a_2 = \frac{1}{3} \quad (27)$$

Using the principle of Tellegen's theorem, R_{loss} for the buck mode is as given in Eq. (28).

$$R_{loss} = \frac{1}{9 * F_{sw}} \left(\frac{1}{C1} + \frac{1}{C2} \right) \quad (28)$$

4. CONVERTER SIMULATION RESULTS

After completing the converter analysis for both no-load and loaded conditions, R_{loss} has been determined for buck and boost modes. The proposed topology for Buck-Boost converter was developed in MATLAB Simulink as presented in Figure 8. It can boost the output voltage level to $2V_{in}$ under no-load conditions. However, when a load is connected to the converter, the output voltage will be reduced, as it is divided between R_{loss} and the load resistor R_L .

The proposed converter is simulated in MATLAB Simulink using the Simscape library. The circuit is modeled using electrical components such as a DC voltage source, resistive load, capacitors, and switching devices. The switches are implemented using ideal switch blocks with a finite on-state resistance to represent non-ideal conduction losses. The non-overlapping clock signals Ph1 and Ph2 are generated using a pulse generator. These signals are applied to the gates of the ideal switches to control their ON and OFF states according to the design.

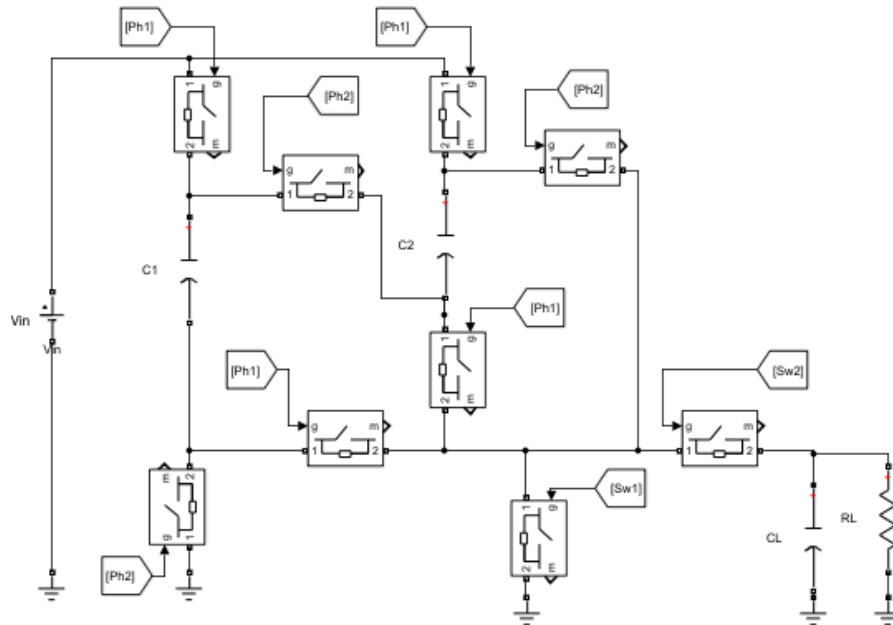


Figure 8. The proposed topology of buck-boost switched-capacitor DC-DC converter

Table 2 and Figure 9 present data for the converter output voltage in boost mode. The input voltage used in this example is 12 V and load resistance is 5 k Ω . At a switching frequency of 600 Hz,

the converter output voltage has been determined to be 18 V instead of 24 V; this reduction due to the effect of the R_{loss} which is calculated from Eq. (21) to be 1.66 k Ω .

The effects of switching on-resistance losses and capacitor charge–discharge losses, can be measured by comparing the converter output voltage under no-load with loaded conditions. The voltage degradation percentage can be computed from Eq. (29).

$$\% \text{ of voltage degradation} = \frac{V_{No-load} - V_{Full-load}}{V_{No-load}} \quad (29)$$

Table 2. Results of converter output voltage for boost mode with different switching frequencies

SF (Hz)	400	600	800	1000	1500	2000	4000	8000
R_L (k Ω)	2.50	1.66	1.25	1.00	0.66	0.50	0.25	0.12
V_O Calculated (V)	16.00	18.00	19.20	20.00	21.17	21.81	22.85	23.41
V_O Simulated (V)	15.60	17.65	18.88	19.73	20.95	21.65	22.70	23.35
V_O Degradation (%)	36.80	29.79	25.22	22.90	20.00	17.50	10.75	7.50

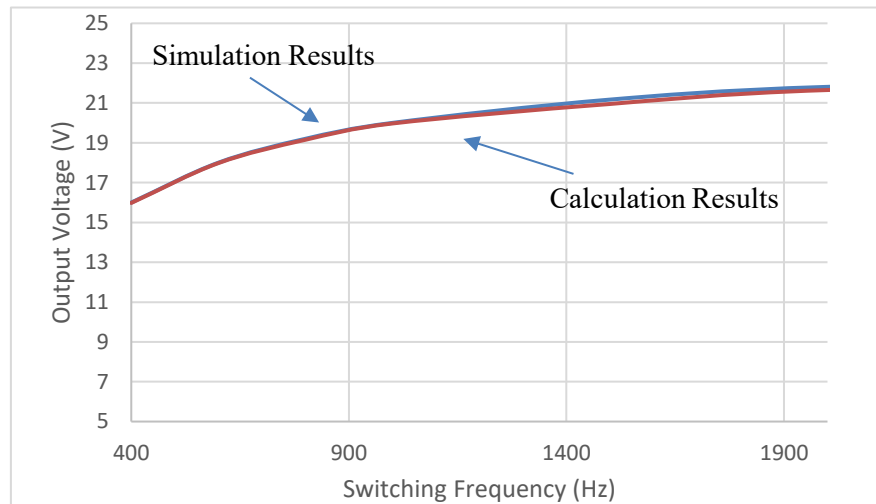


Figure 9. Simulation and calculation results for converter output voltage in boost mode

The output voltage waveforms for the proposed topology of DC-DC converter during boost mode are presented in Figure 10. The waveforms show that as the switching frequency increases, the converter output voltage increases as well. According to Eq. (21), as switching frequency F_{sw} increases, the equivalent resistance R_{loss} decreases, resulting in lower voltage drop across R_{loss} and higher voltage across the load R_L . Also, the converter waveforms in Figure 11 present that as F_{sw} increases, the output voltage ripple decreases because of the shorter switching interval between converter topologies between the converter's topologies. Such important results are clearly highlighted by Figure 11 where zoomed-in views are provided at the transient and steady-state regions.

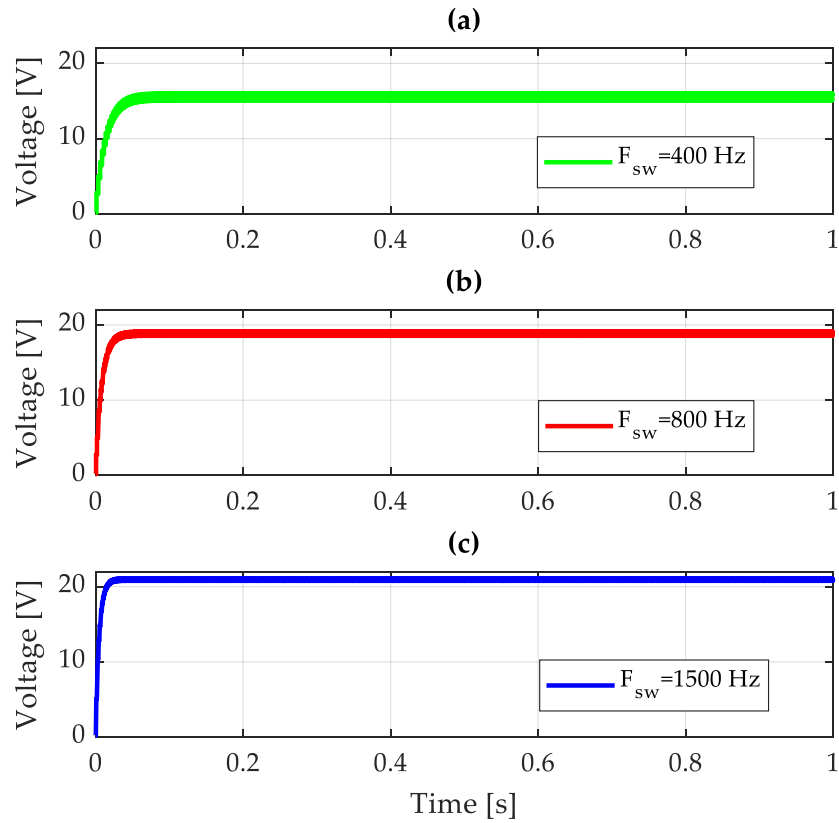


Figure 10. Simulation results of the proposed converter during boost mode with an input voltage of 12 V, a load resistance of 5 k Ω , and switching frequencies F_{sw} (a) 400 Hz (b) 800 Hz (c) 1500 Hz.

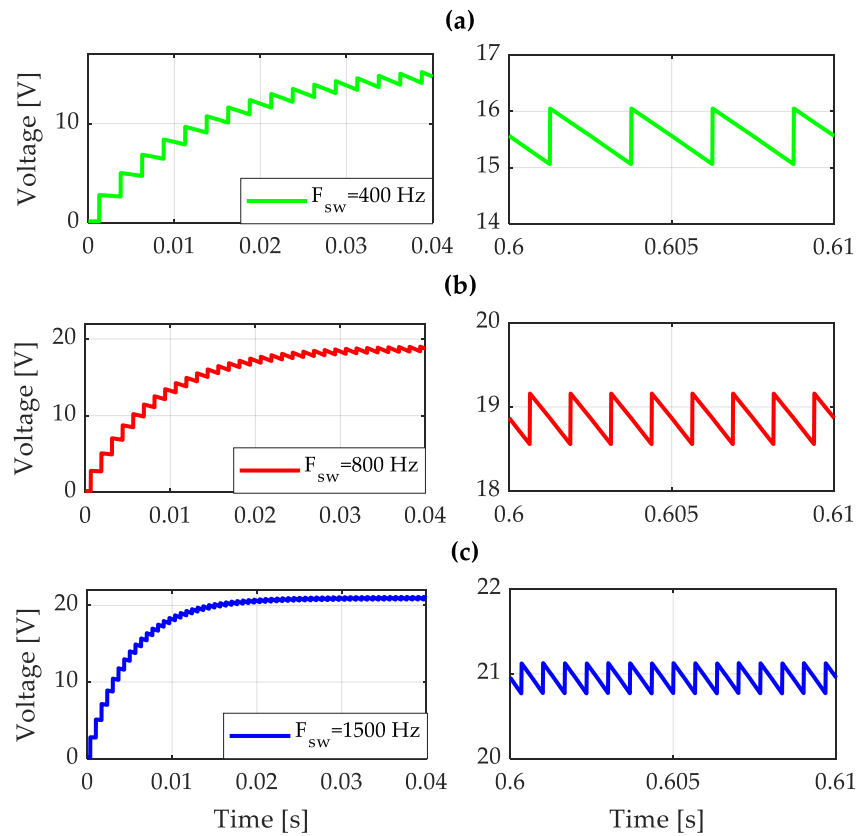


Figure 11. Zoomed region of Figure 10.

The data in table (3), present the converter output voltages for the boost mode at switching frequency equal 700 Hz and input voltage 12V. It shows how the converter responds to different loads. It is clear that as load resistance increases, the converter output voltage increases and gets closer to the ideal output voltage $2V_{in}$ but never reaches it due to R_{loss} .

Table 3. Results of converter output voltage for boost mode with different load resistance

R_L (k Ω)	1	2	5	10	15	20	25	30
V_O Calculation (V)	9.88	14	18.66	21	21.91	22.4	22.7	22.9
V_O Simulation (V)	9.77	13.95	18.65	20.9	21.9	22.38	22.69	22.89

During buck mode, the proposed topology of buck-boost converter is able to step-down the input voltage to $2/3V_{in}$ in case of no load. Yet, the converter actual voltage is less than that due to the effect of the R_{loss} . Table 4 presents the converter output voltages in case of buck mode. For the same example used earlier ($V_{in} = 12V, R_L = 5 K\Omega$), the converter output voltage is 7.71 V at switching frequency of 600 Hz.

Table 4. Results of converter output voltage for buck mode with different switching frequencies

SF (Hz)	400	600	800	1000	1500	2000	4000	8000
R_L (Ω)	277	185	138	110	74	55.5	27.77	13.88
V_O Calculation (V)	7.57	7.71	7.78	7.82	7.88	7.91	7.95	7.98
V_O Simulation (V)	7.65	7.75	7.83	7.85	7.89	7.92	7.95	7.98
V_O Degradation (%)	7.40	7.55	7.63	7.67	7.76	7.79	7.83	7.88

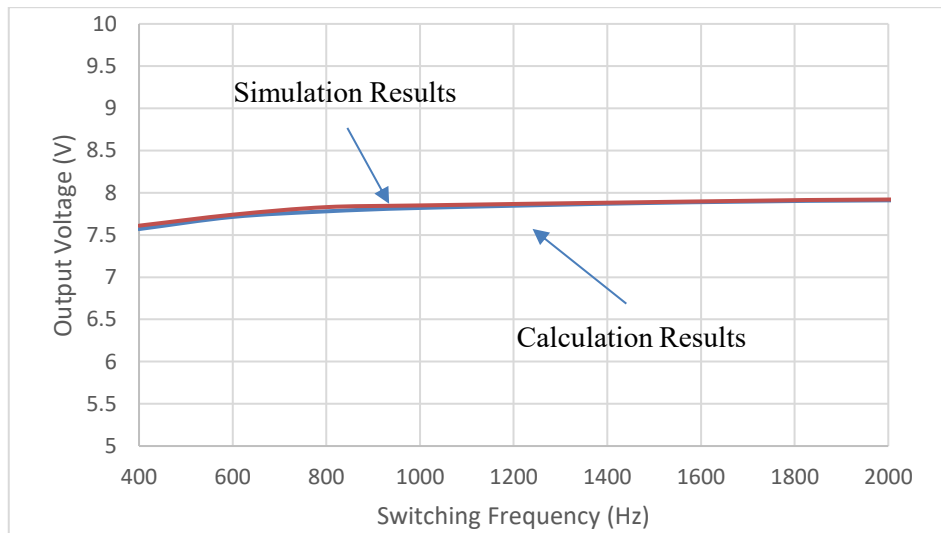


Figure 12. Simulation and Calculation results of converter output voltage during Buck mode

The output voltage waveforms for the proposed topology of DC-DC converter during buck mode are presented in Figures 13 and 14. Referring back to data presented in table 2 and table 4, it is noticeable that the calculated equivalent resistance loss R_{loss} during buck mode is less than boost mode. As a result, the buck mode will reach close to the optimal output voltage of $2/3V_{in}$ faster than boost mode $2V_{in}$.

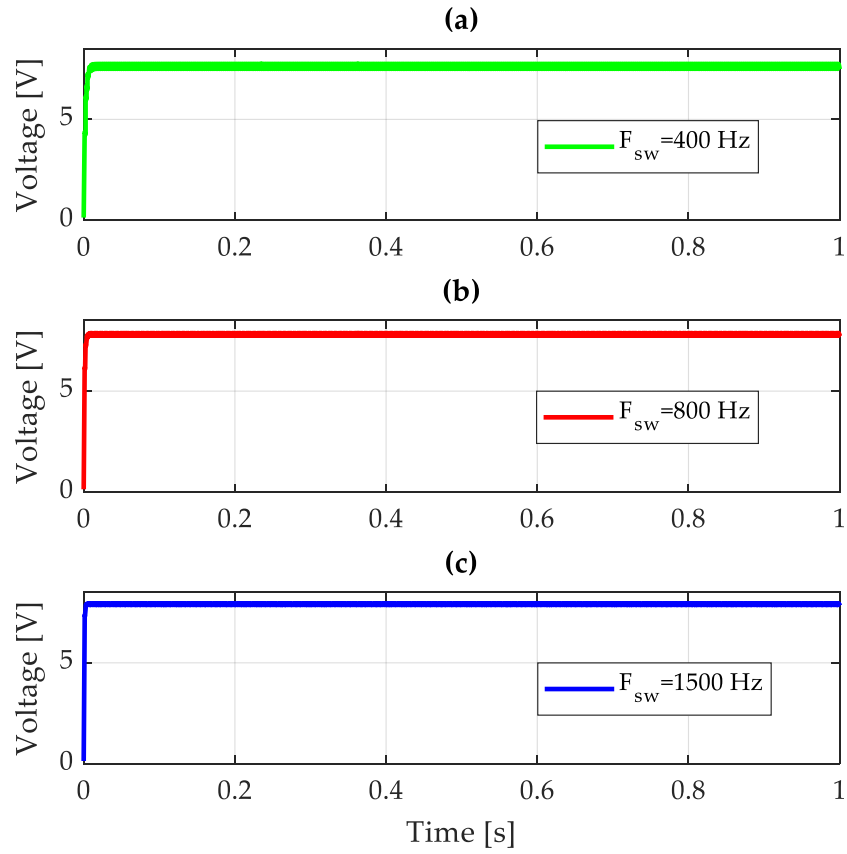


Figure 13. Simulation results of the proposed converter during buck mode with an input voltage of 12 V, a load resistance of 5 k Ω , and switching frequencies F_{sw} (a) 400 Hz (b) 800 Hz (c) 1500 Hz.

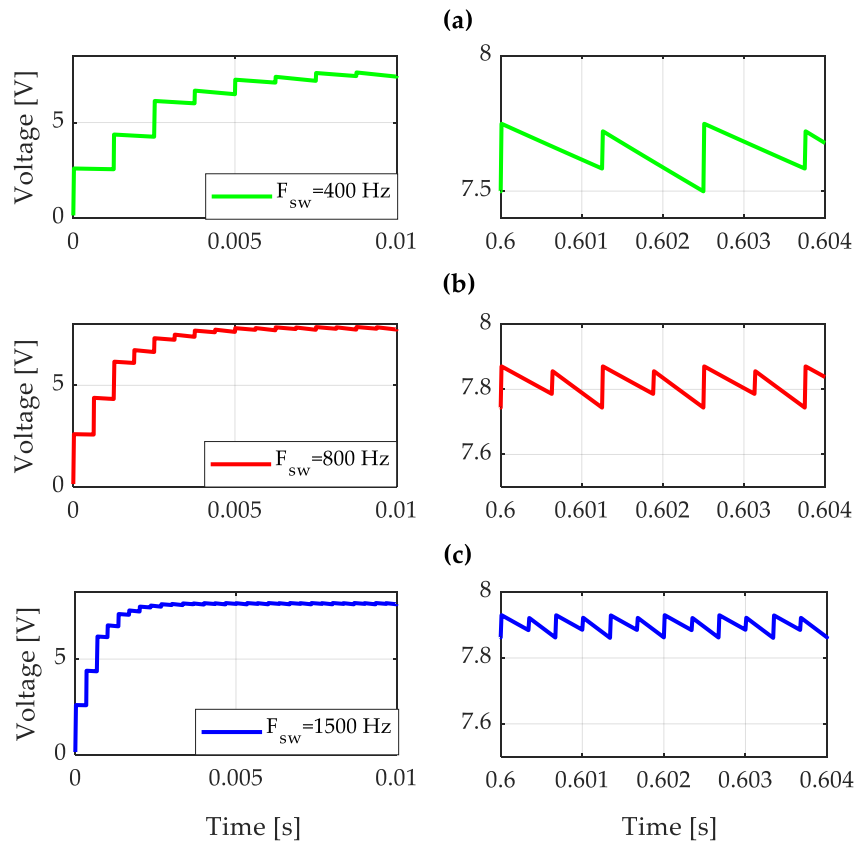


Figure 14. Zoomed region of Figure 13.

The data in table (5) presents the converter's output voltages during buck mode at a switching frequency of 700 Hz and an input voltage of 12V. It illustrates how the converter responds to a variety of load resistances. As R_L increases, the output voltage of the converter rises and approaches the ideal output voltage of $2/3V_{in}$, but it never fully reaches it due to the effect of R_{loss} .

Table 5. Results of converter output voltage for buck mode with different load resistance

R_L (k Ω)	1	2	5	10	15	20	25	30
V_O Calculation (V)	7.02	7.48	7.78	7.89	7.92	7.94	7.95	7.96
V_O Simulation (V)	7.01	7.49	7.79	7.88	7.92	7.94	7.95	7.96

Based on the converter design in section 2, the buck-boost converter can be realized by incorporating two switches into the series and parallel step-down configuration. As shown in Figure 4, the buck mode of the converter is activated by keeping SW1 off and SW2 on continuously. In contrast, the boost mode is triggered by applying a pulse signal V_Ph1 to SW1 and a pulse signal V_Ph2 to SW2.

Table 6. Switch states during buck and boost modes during

Switch	SW1	SW2
Buck	OFF	ON
Boost	V_Ph1	V_Ph2

A key limitation of this design is that the two switches must be individually adjusted to manage the switching process of the converter between buck and boost modes. As a result, it is essential to design an algorithm that allows a single switch to control the converter's mode, activating the buck mode when the switch input is low and the boost mode when the switch input is high (Long et al., 2006). A flowchart of the proposed algorithm to control the switching process is presented in Figure 15.

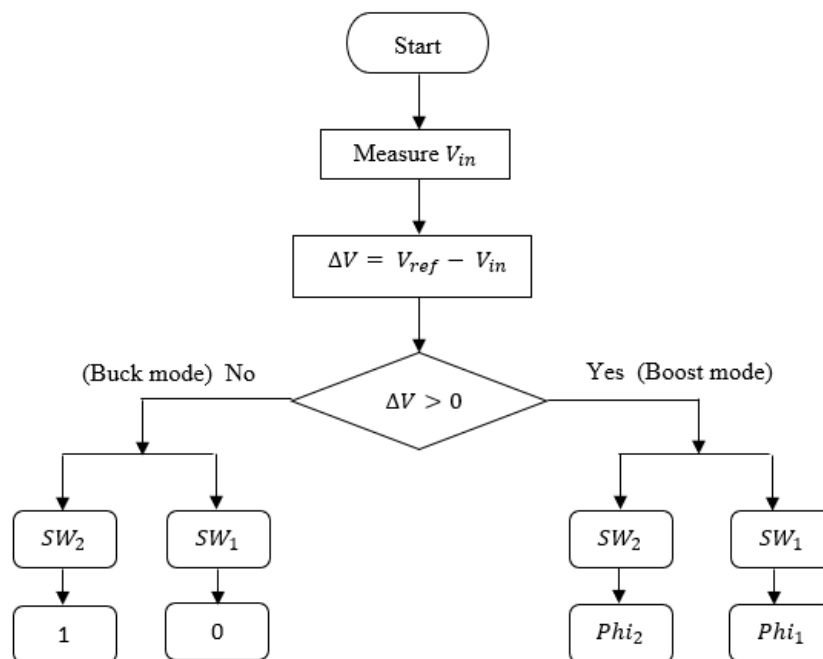


Figure 15. The flowchart for the proposed algorithm to control switching process.

From the switch requirements outlined in Table 6, it is observed that SW1 must remain off during buck mode and activate the pulse signal V_Ph1 during boost mode. On the other hand, SW2 needs to be ON at all times during the buck mode and pass the pulse signal V_Ph2 during the boost mode (Masri and Chan, 2010). These requirements can be implemented with simple comparator logic and logic gates, enabling single-signal mode selection, as presented in Figure 16.

To verify the functionality of applying the proposed algorithm to the buck-boost converter, a load with a constant 5V demand is connected to the converter. The required output voltage is used as the reference voltage; the input voltage is then sensed and compared with this reference as in Figure 16.

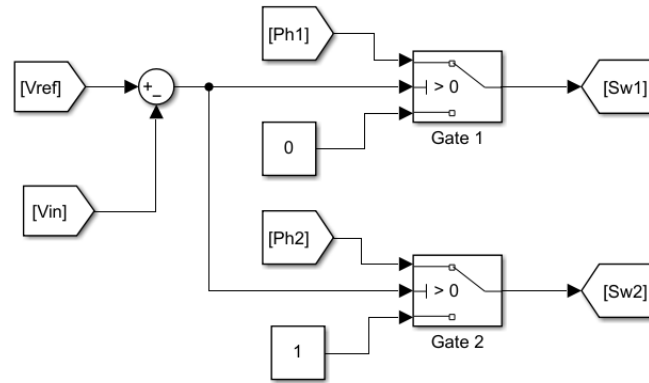


Figure 16. The proposed algorithm to control the converter's switches

The realization of Figure 16 can be carried out using logic gates. For Gate 1, an AND logic gate can be used, while a NAND logic gate can be used for Gate 2. The input signals to the logic gates are the pulse signal Ph1 and the comparator's output signal as shown in Figure 17. The comparator output, represented by a step function, is low in buck mode and high in boost mode. Based on these inputs, the logic circuit generates the required waveform according to the proposed algorithm.

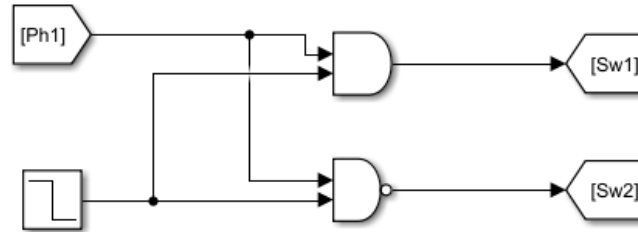


Figure 17. Logic-gate realization of the proposed control algorithm for generating the gate drive signals of SW1 and SW2.

A sweeping voltage is applied to the converter input, ranging from 8 V to 3.5 V. The algorithm waveform presented in Figure 17 shows the result of the proposed control method. During the first half of the simulation period (0–1 s), the input voltage $V_{in} = 8V$ and the reference voltage $V_{ref} = 5V$. In this case, the logic comparator generates a negative signal, which enables the buck mode. The buck mode condition requires that switch SW1 remains OFF and switch SW2 remains ON at all the times. Therefore, during this interval, SW1 is driven by a 0 V signal from gate #1, while SW2 is driven by a 1 V signal from gate #2.

During the second half of the simulation period (1–2 s), the input voltage V_{in} drops to 3.5 V, which is lower than V_{ref} . So, the boost mode is activated, and the logic comparator outputs a positive signal to the gate drivers. In this mode, gate #1 passes the pulse signal V_Ph1 to SW1, while gate #2 passes the pulse signal V_Ph2 to SW2.

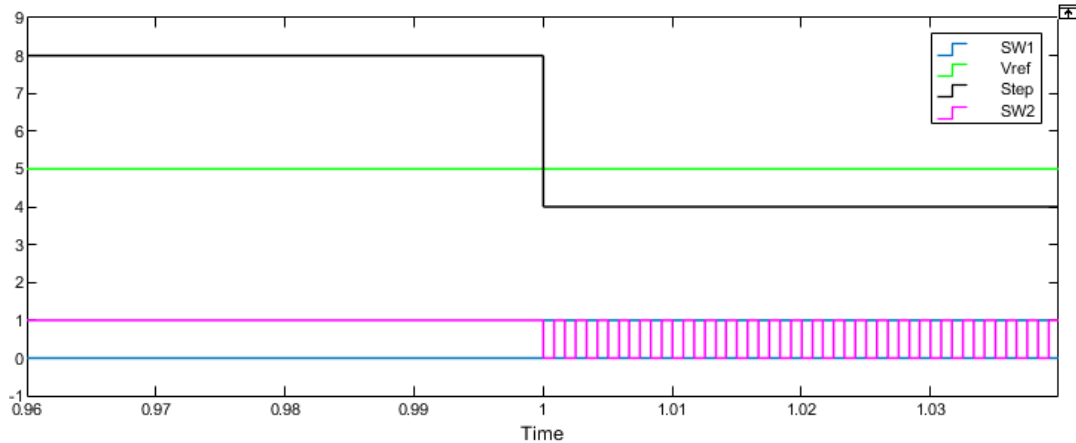


Figure 18. Algorithm outcomes

Figure 19 shows the buck-boost converter response if the input voltage is changing from 8V to 3.5 V at a switching frequency of 600 Hz. When input voltage is 8V, it operates in buck mode which steps the input voltage down to 5V. When the input voltage is 3.5 V, the converter operates in boost mode due to the condition applied, increasing the input voltage to 5V.

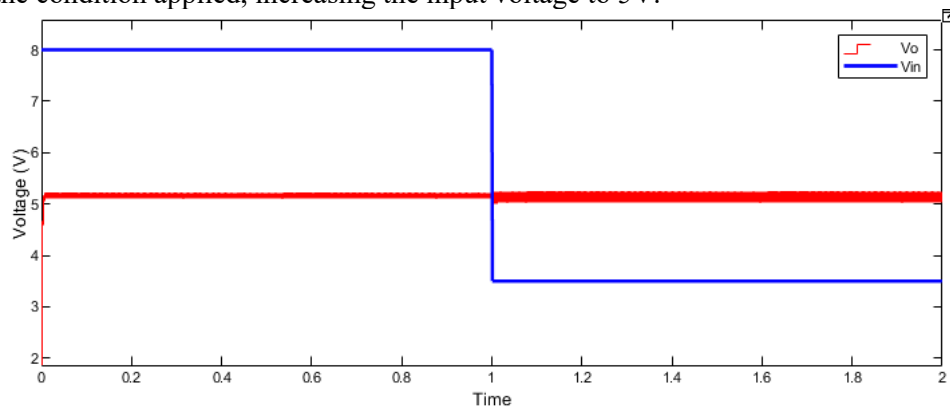


Figure 19. Simulation results of converter output voltage during step-up and step-down modes

Figure 19 presents the simulation results of the proposed converter utilizing the proposed algorithm. The dynamic behavior can be observed from the transient response. It shows that as input voltage changes, the converter transitions directly from buck to boost modes with a smooth response. The output voltage reaches the desired value without noticeable oscillation, indicating stable performance. The response time is controlled by the switching frequency and the charging-discharging rate of the capacitors. A higher switching frequency results in faster dynamic response and reduces voltage ripple. However, the proposed algorithm response is controlled by load conditions and switching frequency. This behavior is consistent with (Pellitteri et al., 2022).

5. CONCLUSION

This paper introduces a novel topology for a buck-boost DC-DC switched-capacitor converter. By incorporating two additional switches into Makowski's step-down topology (Makowski and Maksimovic, 1995), the modified design allows for both step-up and step-down conversion of the input voltage to various output voltage levels. The conversion ratio for the buck-boost converter depends on different parameters and scenarios. In the case of no-load connected to the converter, the conversion ratio is determined by the number of capacitors in the topology. When two charge-transfer capacitors are used in the design, the converter can step-up the input voltage to twice V_{in} and step it down to $2/3$

of Vin. When a load is connected to the converter, its conversion ratio depends on the switching frequency, capacitor values, and load resistance as shown in Eq. (21) and (28).

In this work, Seeman's idealized analytical model (Seeman and Sanders, 2008), was initially selected to establish the theoretical limits of the proposed topology and to simplify the correlation between analytical and simulation results. Future work will include building the proposed topology in the laboratory and incorporating parasitic effects, such as switch on-resistance and capacitor ESR, will be part of future work to quantify efficiency and dynamic performance.

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